DATA SHEET

PCF8579
LCD column driver for dot matrix graphic displays

Product specification
Supersedes data of 1997 Apr 01

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Philips Semiconductors

CONTENTS

1 FEATURES

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40960 dots
- 40 column outputs
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8578)
- Power-on reset blanks display
- Logic voltage supply range 2.5 to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8578)
- Space saving 56-lead plastic mini-pack and 64-pin plastic low profile quad flat package
- Compatible with chip-on-glass technology
- I^2C-bus address: 011110 SA0.

2 APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

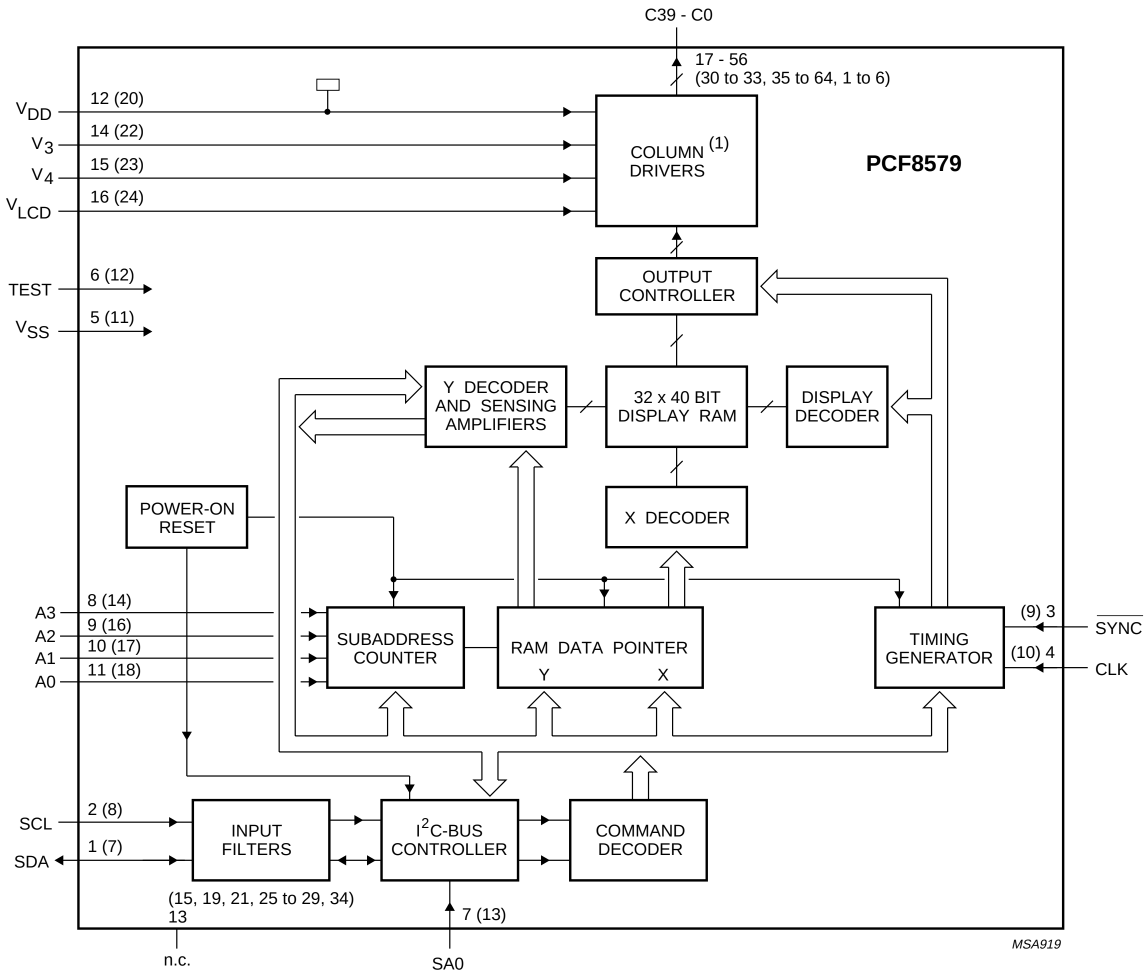
3 GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 × 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}. Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8579H	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
PCF8579T	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8579U	–	chip with bumps on tape	–

5 BLOCK DIAGRAM



(1) Operates at LCD voltage levels, all other blocks operate at logic levels.

The pin numbers given in parenthesis refer to the LQFP64 package.

Fig.1 Block diagram.

6 PINNING

SYMBOL	PINS		DESCRIPTION
	VSO56	LQFP64	
SDA	1	7	I^2C-bus serial data input/output
SCL	2	8	I^2C-bus serial clock input
$\overline{SYNC}$	3	9	cascade synchronization input
CLK	4	10	external clock input
V_{SS}	5	11	ground (logic)
TEST	6	12	test pin (connect to V_{SS})
SA0	7	13	I^2C-bus slave address input (bit 0)
A3 to A0	8 to 11	14, 16 to 18	I^2C-bus subaddress inputs
V_{DD}	12	20	supply voltage
n.c.	13(1)	15, 19, 21,25 to 29, 34	not connected
V_3, V_4	14 and 15	22 and 23	LCD bias voltage inputs
V_{LCD}	16	24	LCD supply voltage
C39 to C0	17 to 56	30 to 33, 35 to 64 and 1 to 6	LCD column driver outputs

Note

1. Do not connect, this pin is reserved.

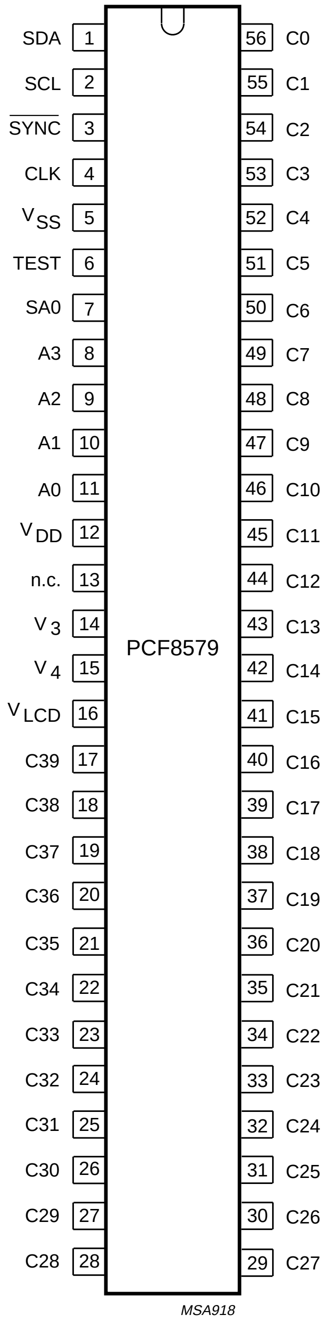


Fig.2 Pin configuration (VSO56).

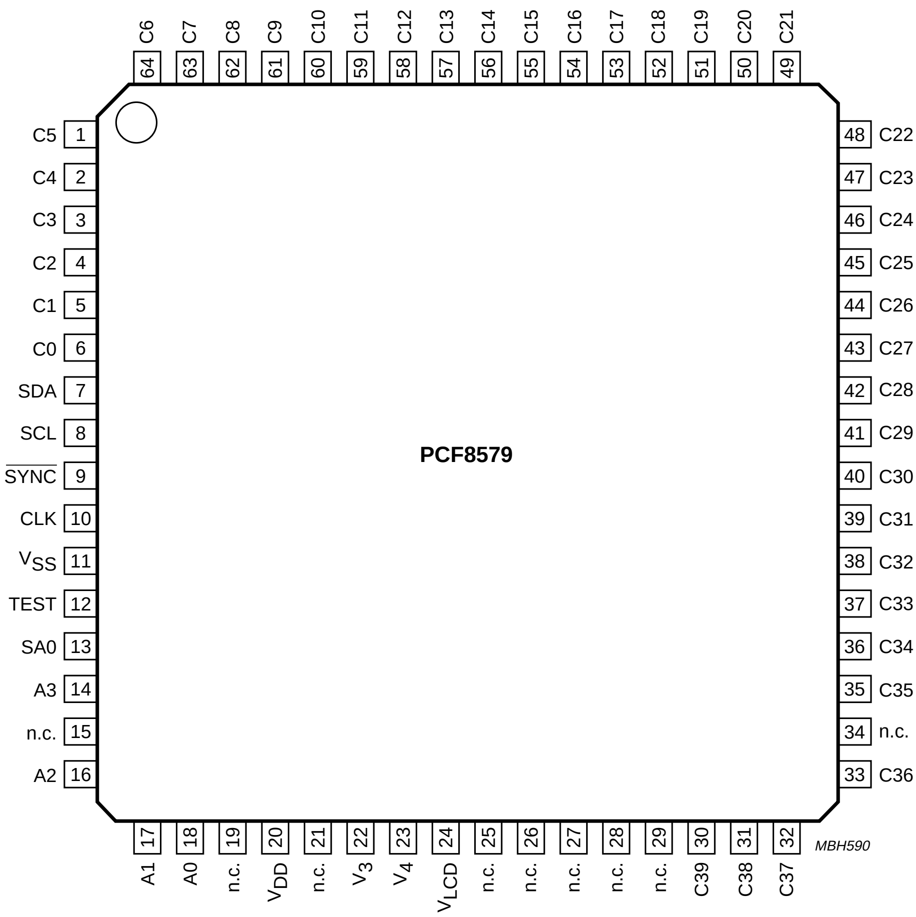


Fig.3 Pin configuration (LQFP64).

7 FUNCTIONAL DESCRIPTION

The PCF8579 column driver is designed for use with the PCF8578. Together they form a general purpose LCD dot matrix chip set.

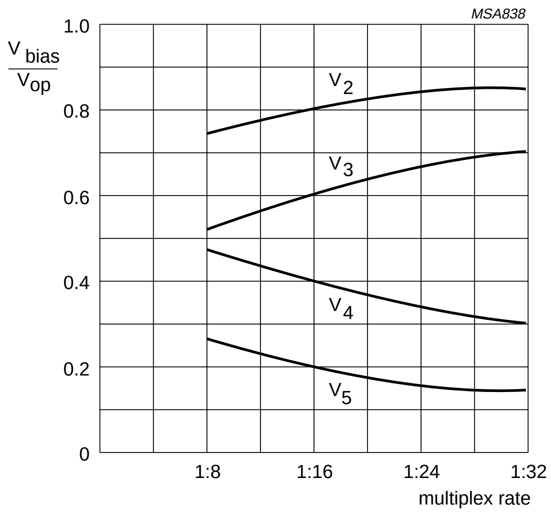
Typically up to 16 PCF8579s may be used with one PCF8578. Each of the PCF8579s is identified by a unique 4-bit hardware subaddress, set by pins A0 to A3.
The PCF8578 can operate with up to 32 PCF8579s when using two I^2C-bus slave addresses. The two slave addresses are set by the logic level on input SA0.

7.1 Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 1 shows the optimum voltage bias levels for the PCF8578/PCF8579 chip set as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}. Figure 4 shows the first 4 rows of Table 1 as graphs.

Table 1 Optimum LCD bias voltages

PARAMETER	MULTIPLEX RATE			
	1 : 8	1 : 16	1 : 24	1 : 32
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.370	4.080	4.680	5.190



$V_{bias} = V_2, V_3, V_4, V_5$. See Table 1.

Fig.4 V_{bias}/V_{op} as a function of the multiplex rate.

7.2 Power-on reset

At power-on the PCF8579 resets to a defined starting condition as follows:

1. Display blank (in conjunction with PCF8578)
2. 1 : 32 multiplex rate
3. Start bank, 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I^2C-bus is initialized.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

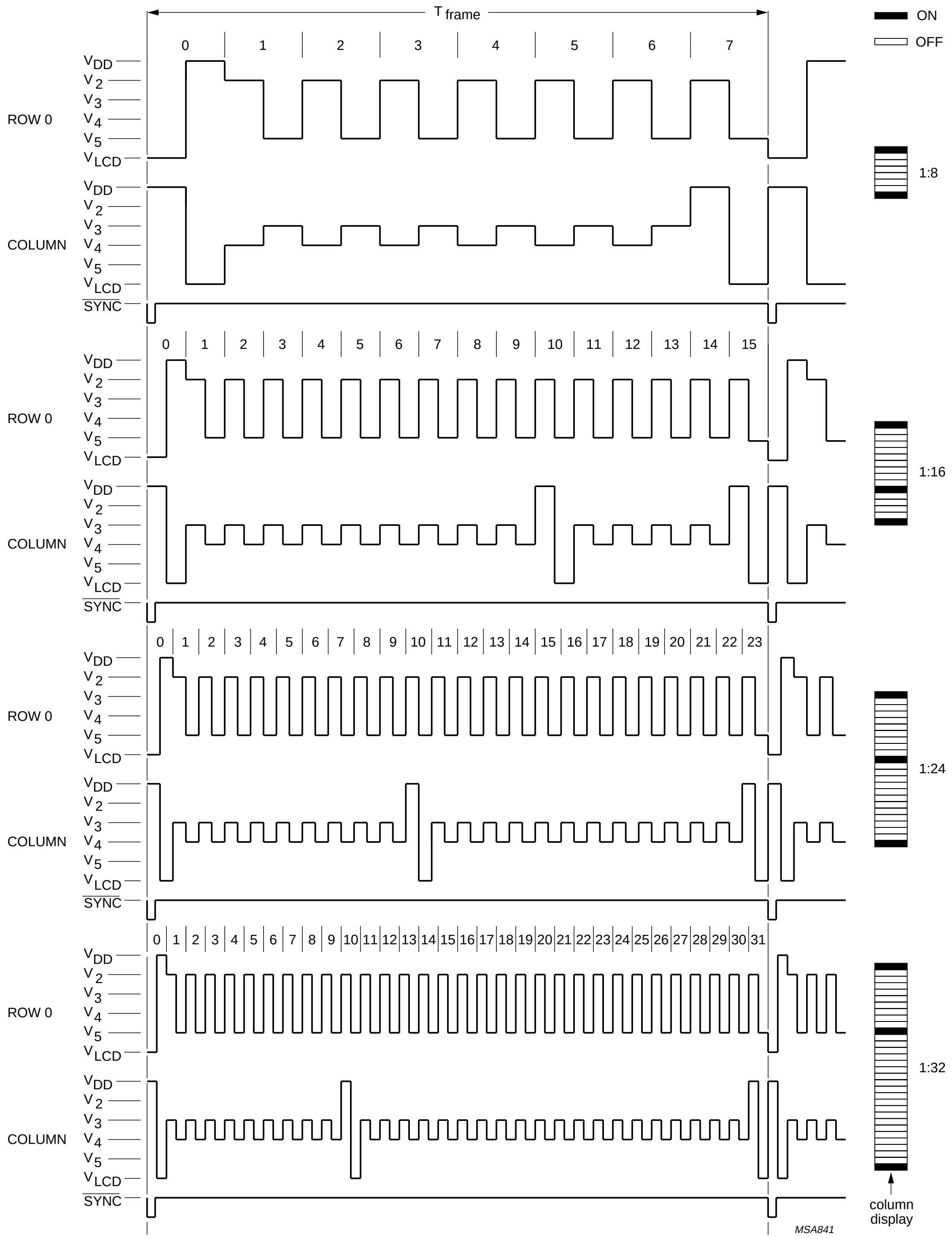
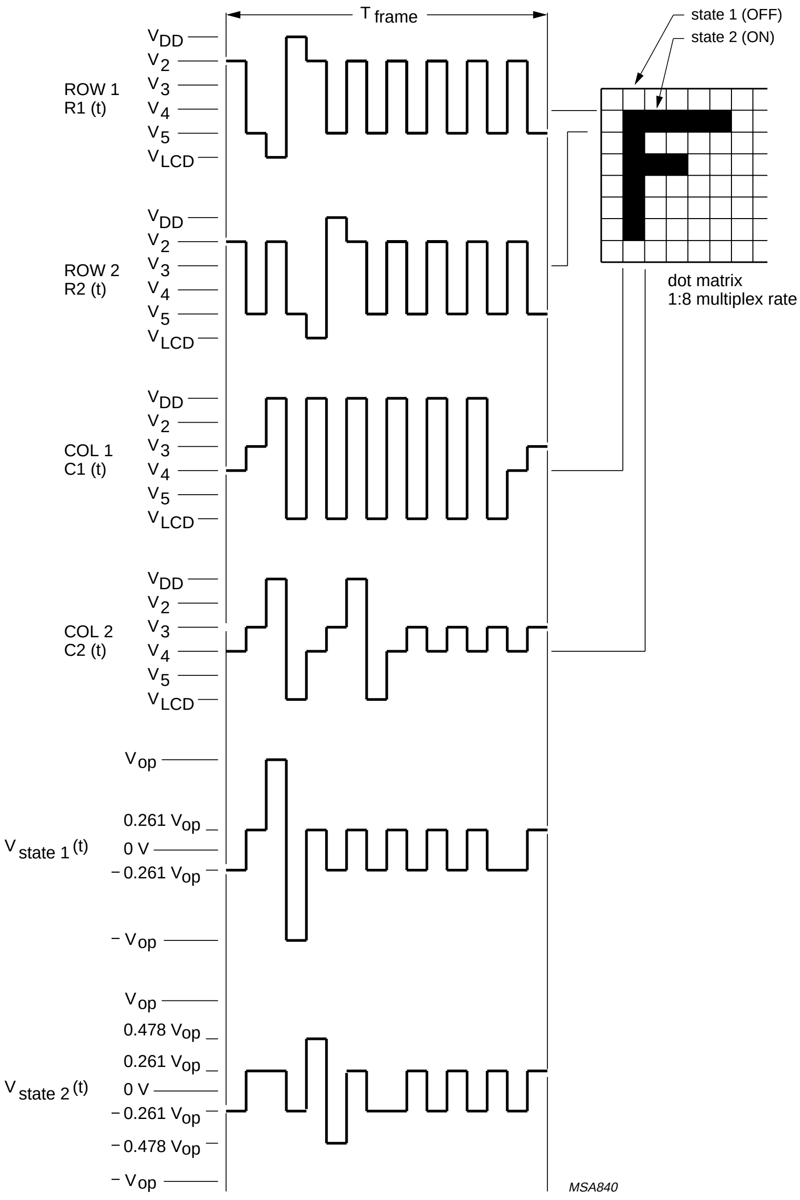


Fig.5 LCD row/column waveforms.



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8} - 1}{8\,(\sqrt{8} + 1)}} = 0.430$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

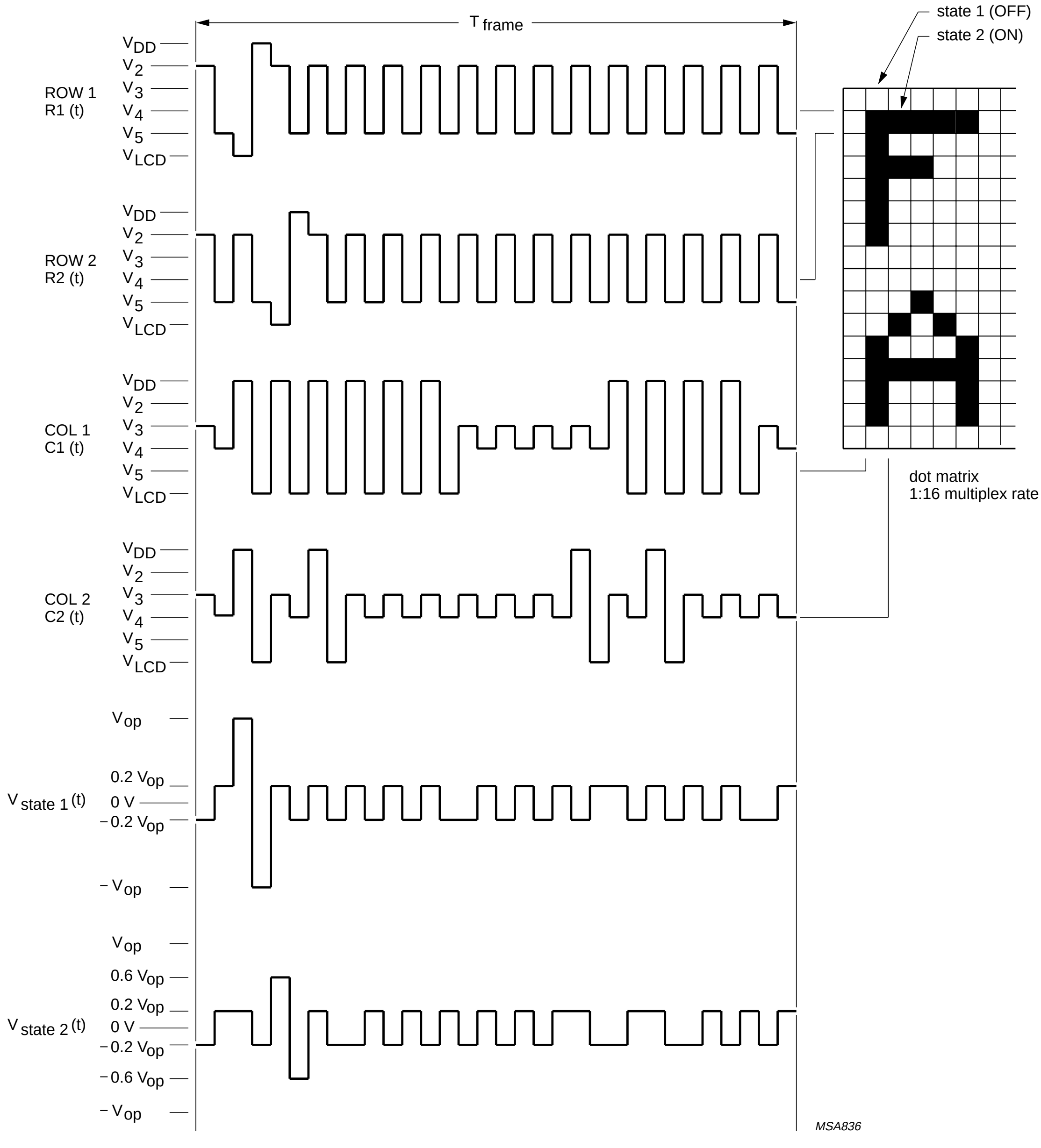
$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{8} - 1)}{\sqrt{8}\,(\sqrt{8} + 1)^2}} = 0.297$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n} - 1}{n\,(\sqrt{n} + 1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n} - 1)}{\sqrt{n}\,(\sqrt{n} + 1)^2}}$$

Fig.6 LCD drive mode waveforms for 1 : 8 multiplex rate.



$V_{state\ 1}$ (t) = C1(t) − R1(t):

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16} - 1}{16\,(\sqrt{16} + 1)}} = 0.316$$

$V_{state\ 2}$ (t) = C2(t) − R2(t):

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{16} - 1)}{\sqrt{16}\,(\sqrt{16} + 1)^2}} = 0.254$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n} - 1}{n\,(\sqrt{n} + 1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n} - 1)}{\sqrt{n}\,(\sqrt{n} + 1)^2}}$$

Fig.7 LCD drive mode waveforms for 1 : 16 multiplex rate.sa.

7.3 Timing generator

The timing generator of the PCF8579 organizes the internal data flow from the RAM to the display drivers. An external synchronization pulse $\overline{SYNC}$ is received from the PCF8578. This signal maintains the correct timing relationship between cascaded devices.

7.4 Column drivers

Outputs C0 to C39 are column drivers which must be connected to the LCD. Unused outputs should be left open-circuit.

7.5 Display RAM

The PCF8579 contains a 32 × 40-bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes (4 × 8 × 40 bits). During RAM access, data is transferred to/from the RAM via the I^2C-bus.

7.6 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into, or read from, the display RAM, controlled by commands sent on the I^2C-bus.

7.7 Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage and retrieval take place only when the contents of the subaddress counter agree with the hardware subaddress at pins A0, A1, A2 and A3.

7.8 I^2C-bus controller

The I^2C-bus controller detects the I^2C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8579 acts as an I^2C-bus slave transmitter/receiver. Device selection depends on the I^2C-bus slave address, the hardware subaddress and the commands transmitted.

7.9 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.10 RAM access

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic.

These modes are specified by bits G1 and G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.8).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.9):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command).

Subsequent data bytes will be written or read according to the chosen RAM access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

7.11 Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.10 This feature is useful when scrolling in alphanumeric applications.

7.12 TEST pin

The TEST pin must be connected to V_{SS}.

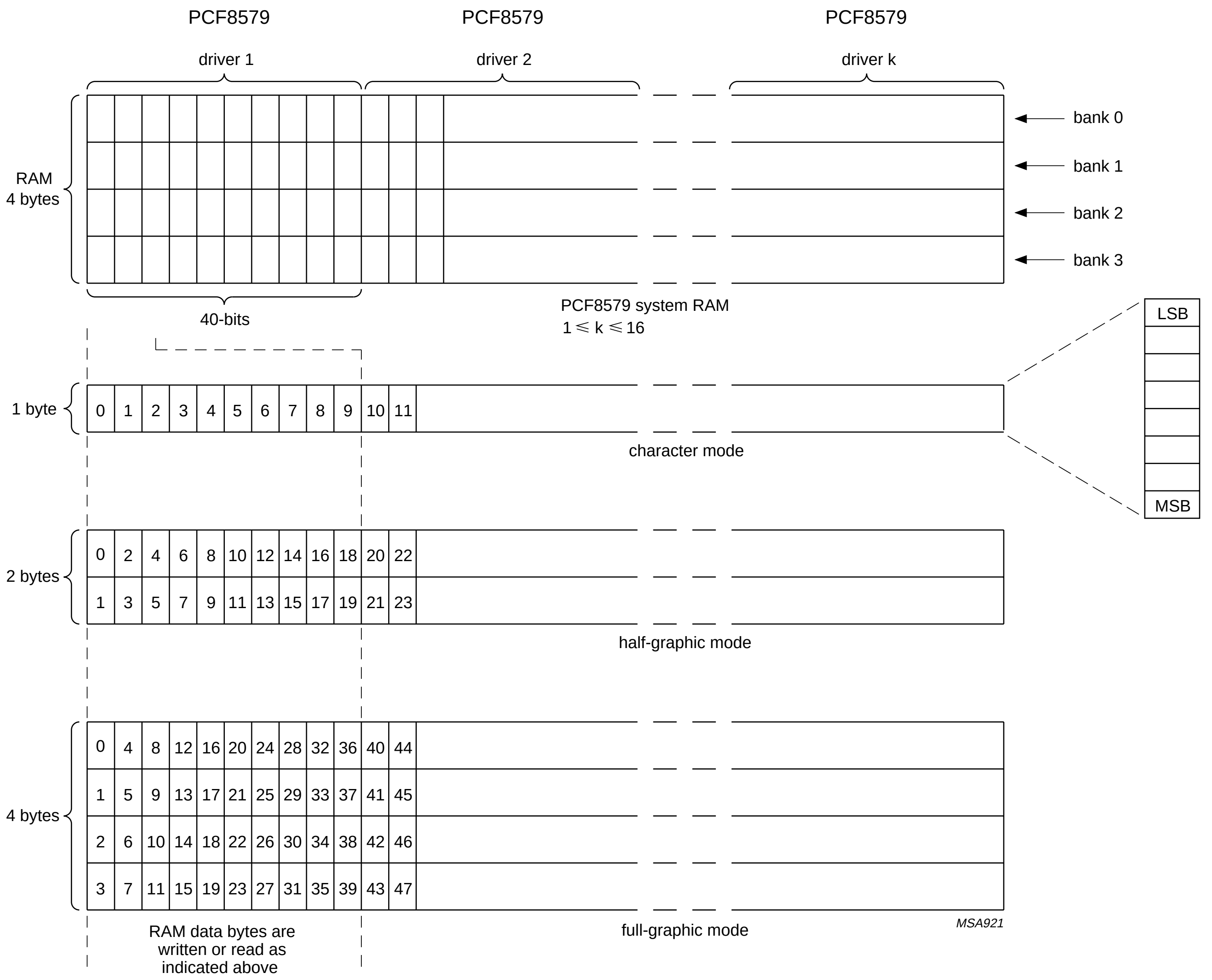


Fig.8 RAM access mode.

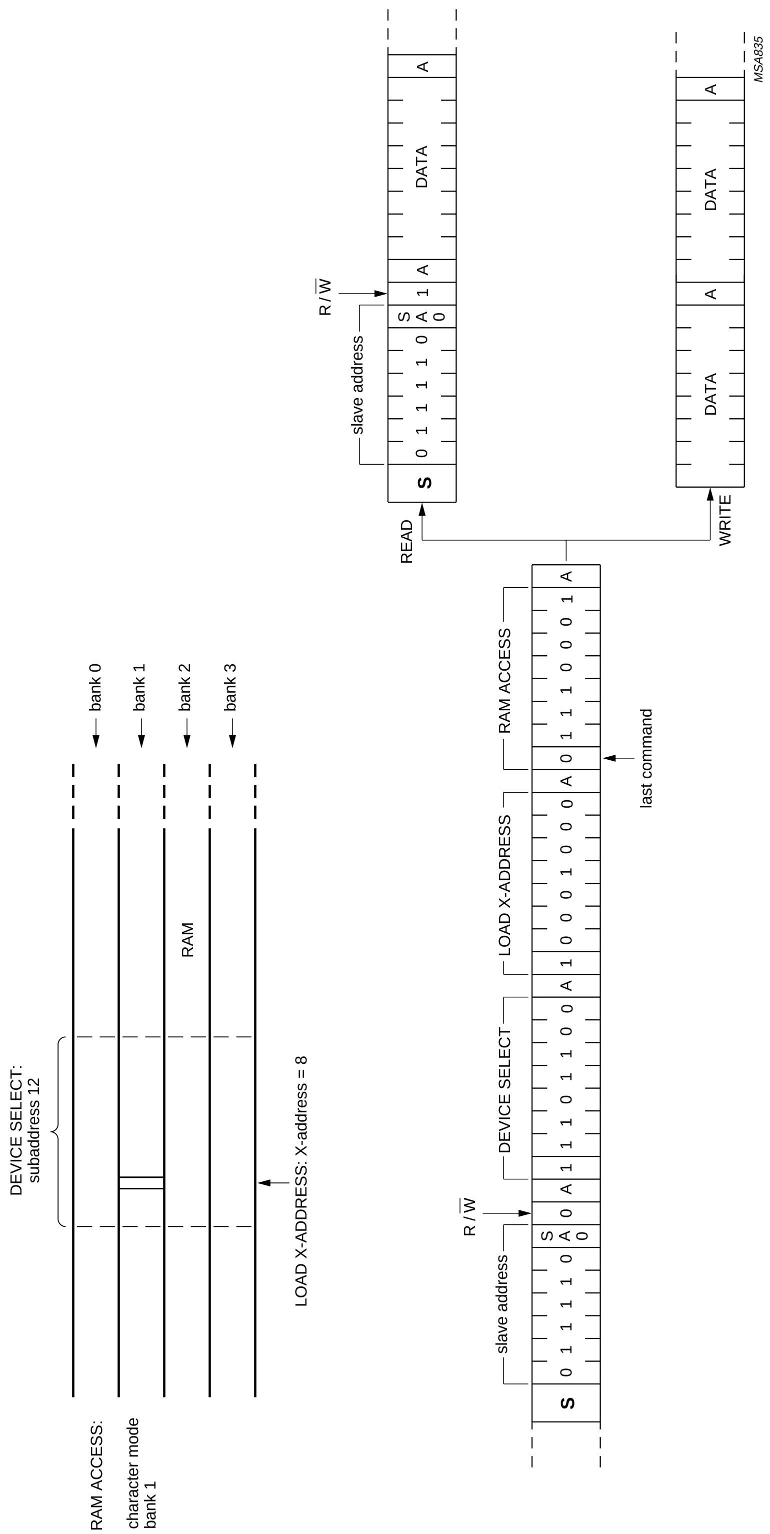


Fig.9 Example of commands specifying initial data byte RAM locations.

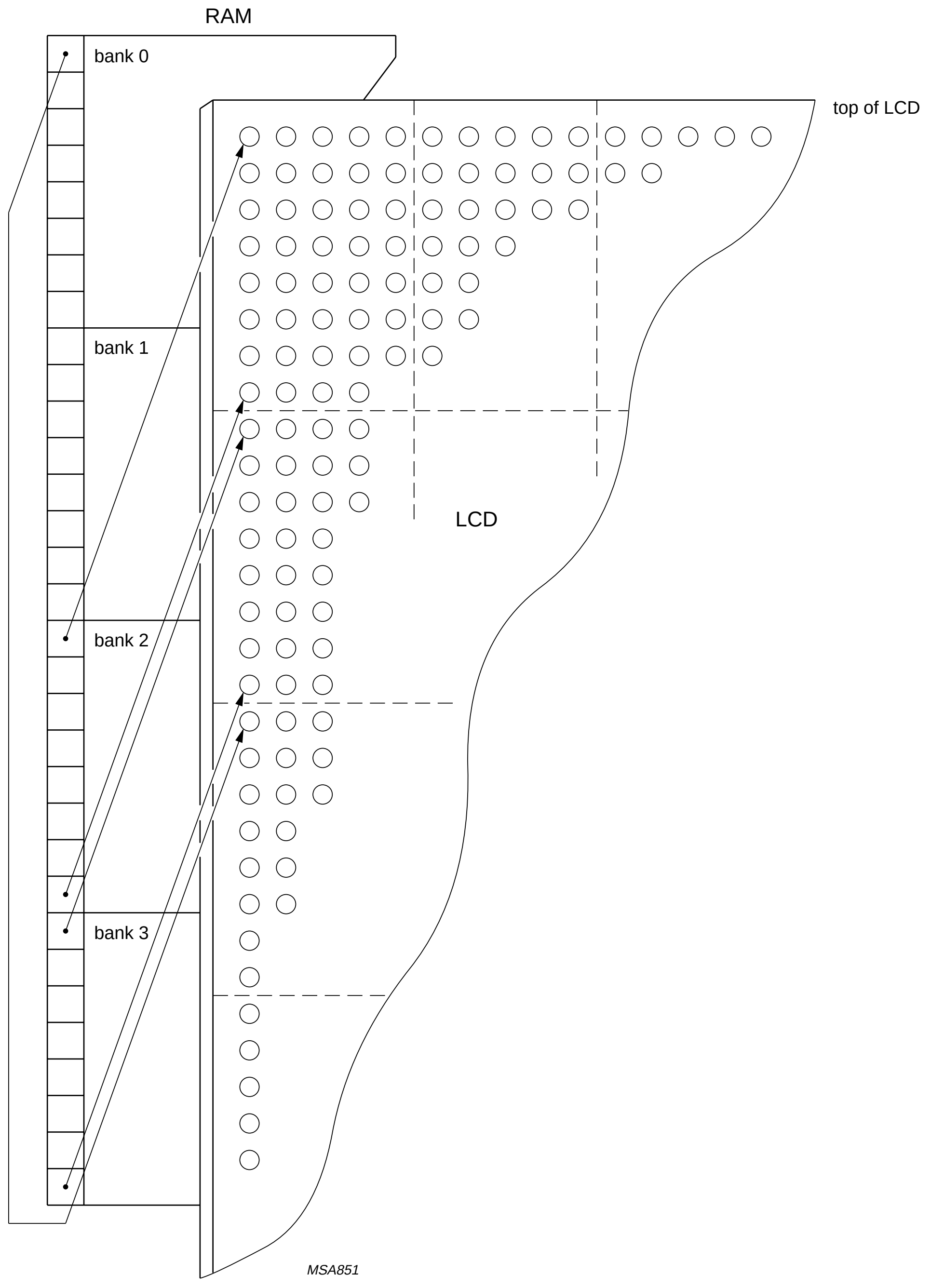


Fig.10 Relationship between display and SET START BANK; 1 : 32 multiplex rate and start bank = 2.

8 I^2C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least significant bit of the slave address is set by connecting input SA0 to either logic 0 (V_{SS}) or logic 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I^2C-bus which allows:

1. One PCF8578 to operate with up to 32 PCF8579s on the same I^2C-bus for very large applications.
2. The use of two types of LCD multiplex schemes on the same I^2C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I^2C-bus protocol is shown in Fig.11.
All communications are initiated with a start condition (S) from the I^2C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus.
The last command must clear the continuation bit C. After the last command a series of data bytes may follow.
The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I^2C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8579 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by **not** generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A0 to A3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated a unique hardware subaddress.

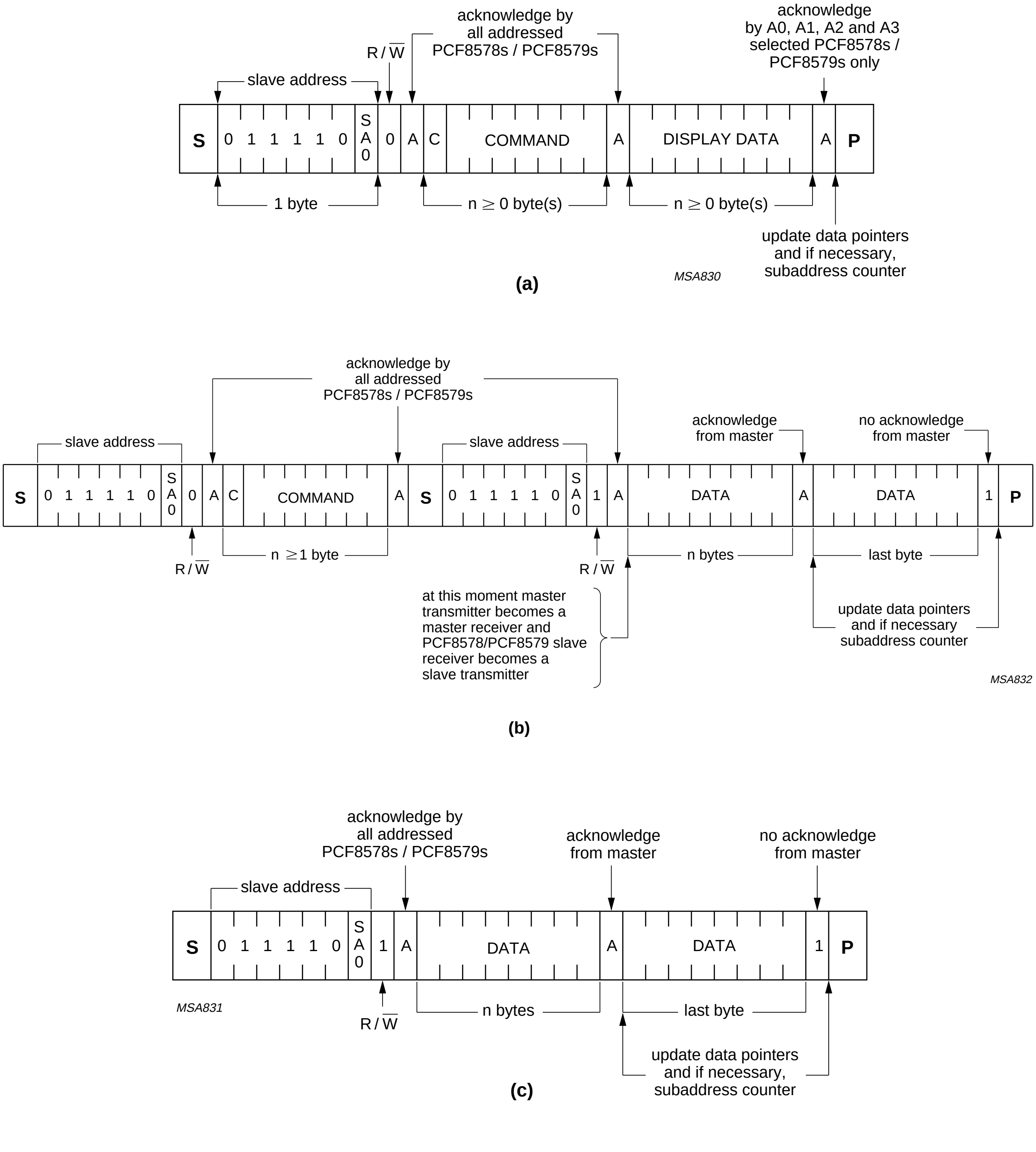
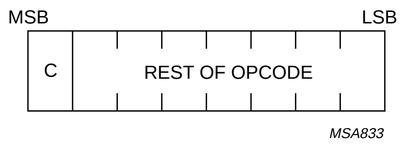


Fig.11 (a) Master transmits to slave receiver (WRITE mode); (b) Master reads after sending command string (WRITE commands; READ data); (c) Master reads slave immediately after sending slave address (READ mode).

8.1 Command decoder

The command decoder identifies command bytes that arrive on the I^2C-bus. The most significant bit of a command is the continuation bit C (see Fig.12). When this bit is set, it indicates that the next byte to be transferred will also be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.

The five commands available to the PCF8579 are defined in Tables 2 and 3.



C = 0; last command.
C = 1; commands continue.

Fig.12 General format of command byte.

Table 2 Summary of commands

COMMAND	OPCODE[1]								DESCRIPTION
SET MODE	C	1	0	D	D	D	D	D	multiplex rate, display status, system type
SET START BANK	C	1	1	1	1	1	D	D	defines bank at top of LCD
DEVICE SELECT	C	1	1	0	D	D	D	D	defines device subaddress
RAM ACCESS	C	1	1	1	D	D	D	D	graphic mode, bank select (D D D D ≥ 12 is not allowed; see SET START BANK opcode)
LOAD X-ADDRESS	C	0	D	D	D	D	D	D	0 to 39

Note

1. C = command continuation bit. D = may be a logic 1 or 0.

Table 3 Definition of PCF8578/PCF8579 commands

COMMAND	OPCODE								OPTIONS	DESCRIPTION
SET MODE	C	1	0	T	E1	E0	M1	M0	see Table 4	defines LCD drive mode
									see Table 5	defines display status
									see Table 6	defines system type
SET START BANK	C	1	1	1	1	1	B1	B0	see Table 7	defines pointer to RAM bank corresponding to the top of the LCD; useful for scrolling, pseudo motion and background preparation of new display
DEVICE SELECT	C	1	1	0	A3	A2	A1	A0	see Table 8	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses
RAM ACCESS	C	1	1	1	G1	G0	Y1	Y0	see Table 9	defines the auto-increment behaviour of the address for RAM access
									see Table 10	two bits of immediate data, bits Y0 to Y1, are transferred to the X-address pointer to define one of forty display RAM columns
LOAD X-ADDRESS	C	0	X5	X4	X3	X2	X1	X0	see Table 11	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

Table 4 Set mode option 1

LCD DRIVE MODE		BITS	
		M1	**M0**
1 : 8	MUX (8 rows)	0	1
1 : 16	MUX (16 rows)	1	0
1 : 24	MUX (24 rows)	1	1
1 : 32	MUX (32 rows)	0	0

Table 5 Set mode option 2

DISPLAY STATUS	BITS	
	E1	**E0**
Blank	0	0
Normal	0	1
All segments on	1	0
Inverse video	1	1

Table 6 Set mode option 3

SYSTEM TYPE	BIT T
PCF8578 row only	0
PCF8578 mixed mode	1

Table 7 Set start bank option 1

START BANK POINTER	BITS	
	B1	**B0**
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1

Table 8 Device select option 1

DESCRIPTION	BITS			
Decimal value of 0 to 15	A3	A2	A1	A0

Table 9 RAM access option 1

RAM ACCESS MODE	BITS	
	G1	**G0**
Character	0	0
Half-graphic	0	1
Full-graphic	1	0
Not allowed (note 1)	1	1

Note

1. See opcode for SET START BANK in Table 3.

Table 10 RAM access option 2

DESCRIPTION	BITS	
Decimal value of 0 to 3	Y1	Y0

Table 11 Load X-address option 1

DESCRIPTION	BITS					
Decimal value of 0 to 39	X5	X4	X3	X2	X1	X0

9 CHARACTERISTICS OF THE I^{2}C-BUS

The I^{2}C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse.
The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

9.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S).
A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

9.3 System configuration

A device transmitting a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message flow is the 'master' and the devices which are controlled by the master are the 'slaves'.

9.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.
A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

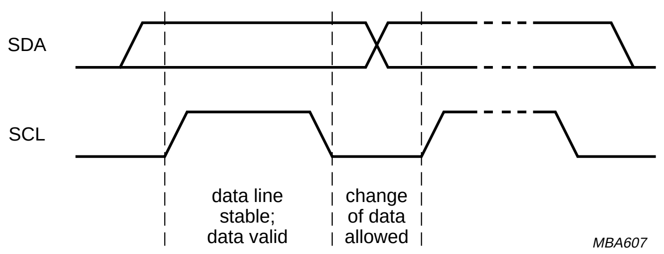


Fig.13 Bit transfer.

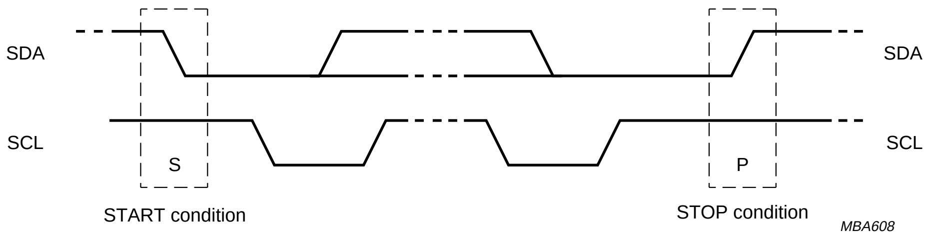


Fig.14 Definition of start and stop condition.

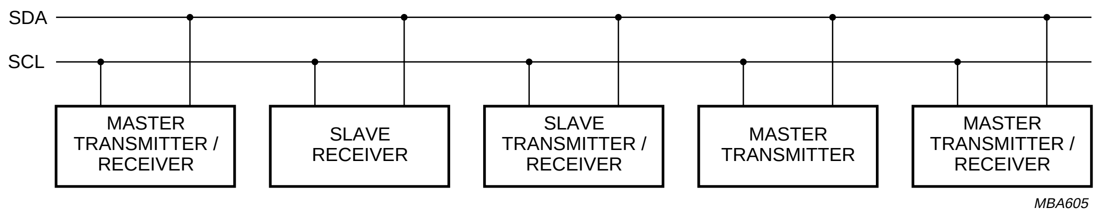
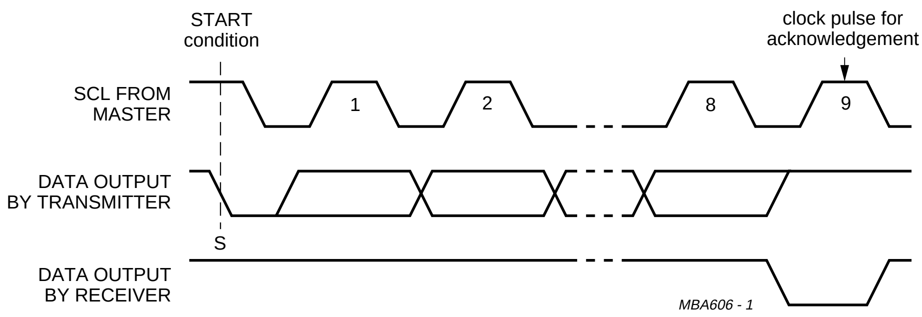


Fig.15 System configuration.



The general characteristics and detailed specification of the I^{2}C-bus are available on request.

Fig.16 Acknowledgement on the I^{2}C-bus.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} – 11	V_{DD}	V
V_{i1}	input voltage pins SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_{SS} – 0.5	V_{DD} + 0.5	V
V_{i2}	input voltage pins V_3 and V_4	V_{LCD} – 0.5	V_{DD} + 0.5	V
V_{o1}	output voltage pin SDA	V_{SS} – 0.5	V_{DD} + 0.5	V
V_{o2}	output voltage pins C0 to C39	V_{LCD} – 0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	current at pins V_{DD}, V_{SS} or V_{LCD}	–50	+50	mA
P_{tot}	total power dissipation per package	–	400	mW
P_o	power dissipation per output	–	100	mW
T_{stg}	storage temperature	–65	+150	°C

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *“Handling MOS Devices”.*

12 DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; $V_{LCD} = V_{DD} - 3.5$ V to $V_{DD} - 9$ V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.5	–	6.0	V
V_{LCD}	LCD supply voltage		$V_{DD} - 9$	–	$V_{DD} - 3.5$	V
I_{DD}	supply current	f_{CLK} = 2 kHz; note 1	–	9	20	μA
V_{POR}	power-on reset level	note 2	–	1.3	1.8	V
Logic						
V_{IL}	LOW level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI1}	leakage current at pins SDA, SCL, $\overline{\text{SYNC}}$, CLK, TEST, SA0, A0, A1, A2 and A3	$V_i = V_{DD}$ or V_{SS}	–1	–	+1	μA
I_{OL}	LOW level output current at pin SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
C_i	input capacitance	note 3	–	–	5	pF
LCD outputs						
I_{LI2}	leakage current at pins V_3 to V_4	$V_i = V_{DD}$ or V_{LCD}	–2	–	+2	μA
V_{DC}	DC component of LCD drivers pins C0 to C39		–	±20	–	mV
R_{COL}	output resistance at pins C0 to C39	note 4	–	3	6	kΩ

Notes

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; clock with 50% duty factor.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (C0 to C39) and bias input (V_3, V_4, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 1):
   a) – $V_{op} = V_{DD} - V_{LCD}$ = 9 V;
   b) – $V_3 - V_{LCD} \geq 4.70$ V; $V_4 - V_{LCD} \leq 4.30$ V; I_{LOAD} = 100 μA.

13 AC CHARACTERISTICS

All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} – 3.5 V to V_{DD} – 9 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clk}	clock frequency	50% duty factor	–	note 1	10	kHz
t_{PLCD}	driver delays	V_{DD} – V_{LCD} = 9 V; with test loads	–	–	100	μs
I²C-bus						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SW}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	μs
$t_{SU;STA}$	START condition set-up time	repeated start codes only	4.7	–	–	μs
$t_{HD;STA}$	START condition hold time		4.0	–	–	μs
t_{LOW}	SCL LOW time		4.7	–	–	μs
t_{HIGH}	SCL HIGH time		4.0	–	–	μs
t_r	SCL and SDA rise time		–	–	1.0	μs
t_f	SCL and SDA fall time		–	–	0.3	μs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	μs

Note

1. Typically 0.9 to 3.3 kHz.

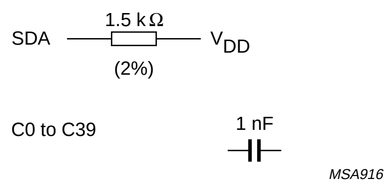


Fig.17 AC test loads.

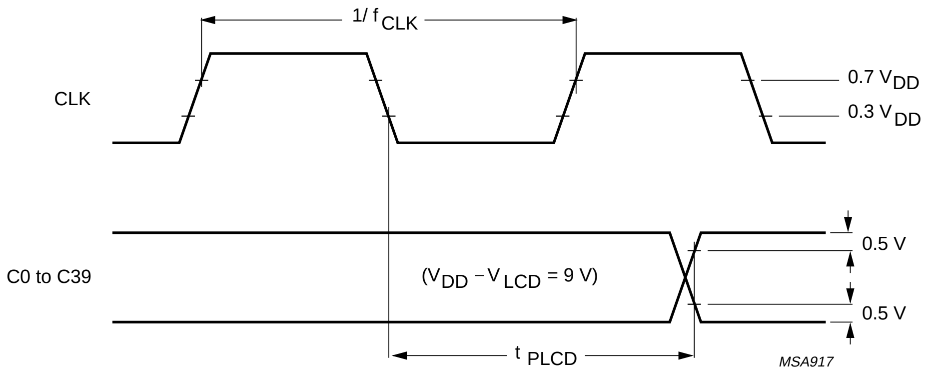


Fig.18 Driver timing waveforms.

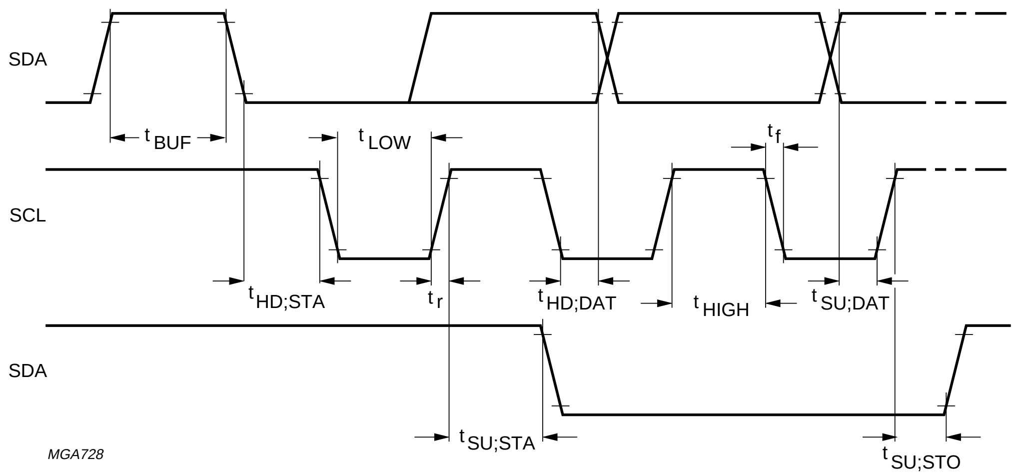


Fig.19 I^2C-bus timing waveforms.

14 APPLICATION INFORMATION

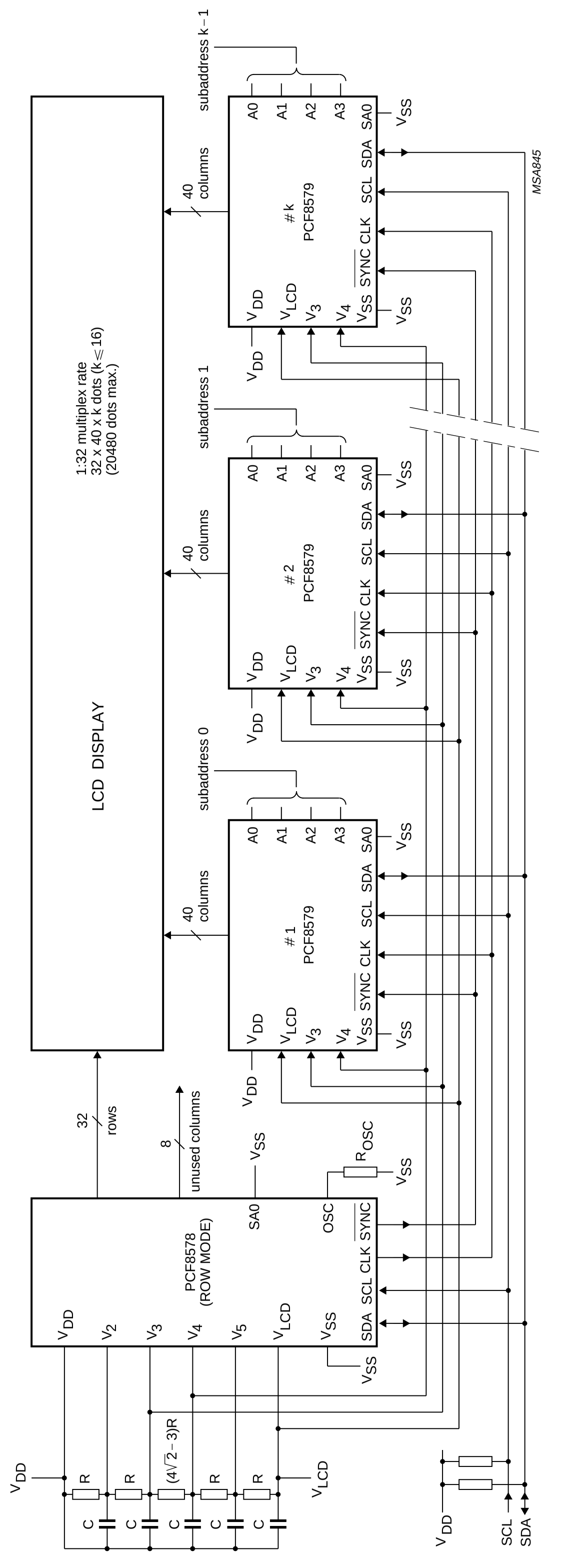


Fig.20 Typical LCD driver system with 1 : 32 multiplex rate.

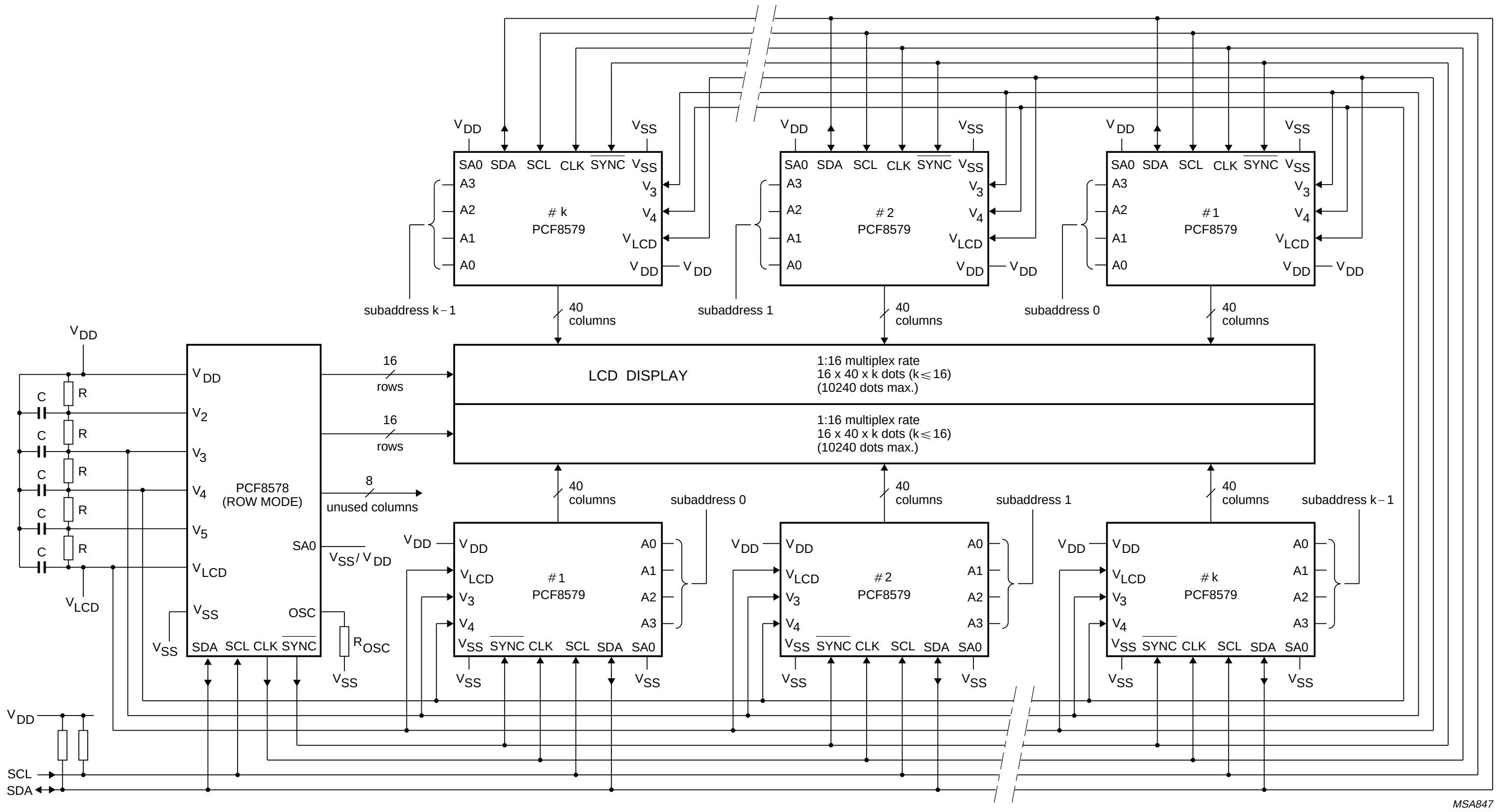


Fig.21 Split screen application with 1 : 16 multiplex rate for improved contrast.

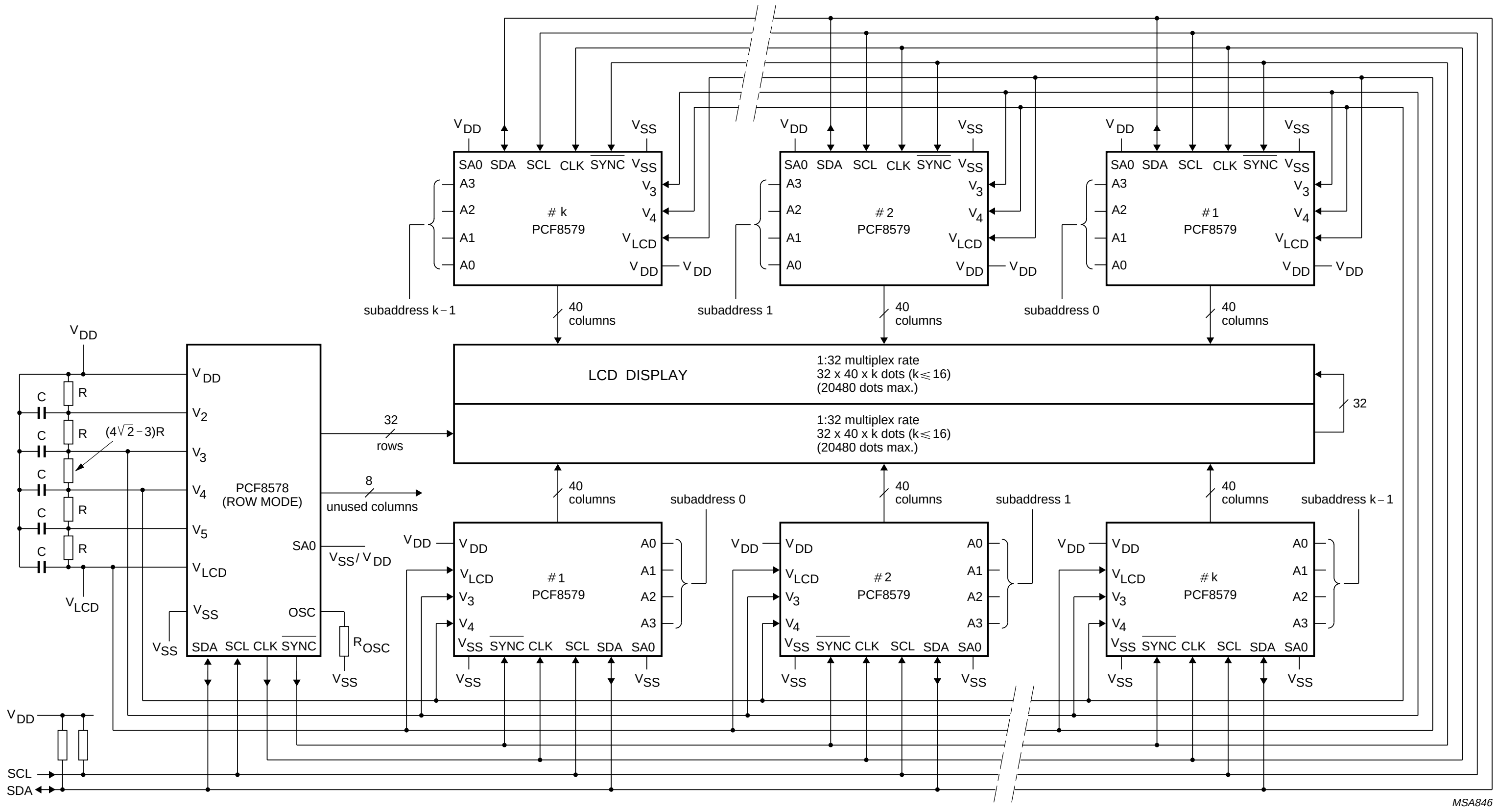


Fig.22 Split screen application with 1 : 32 multiplex rate.

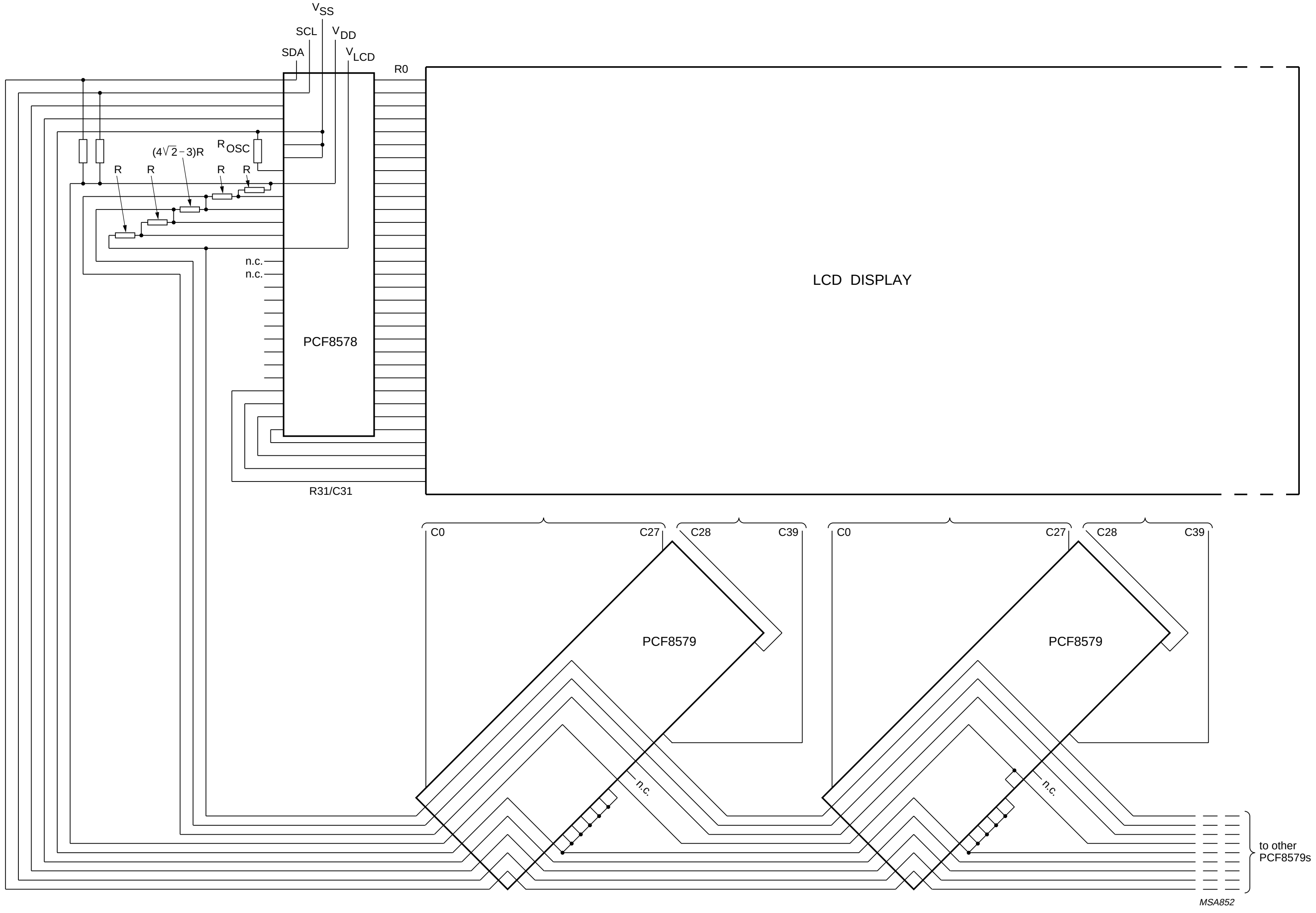
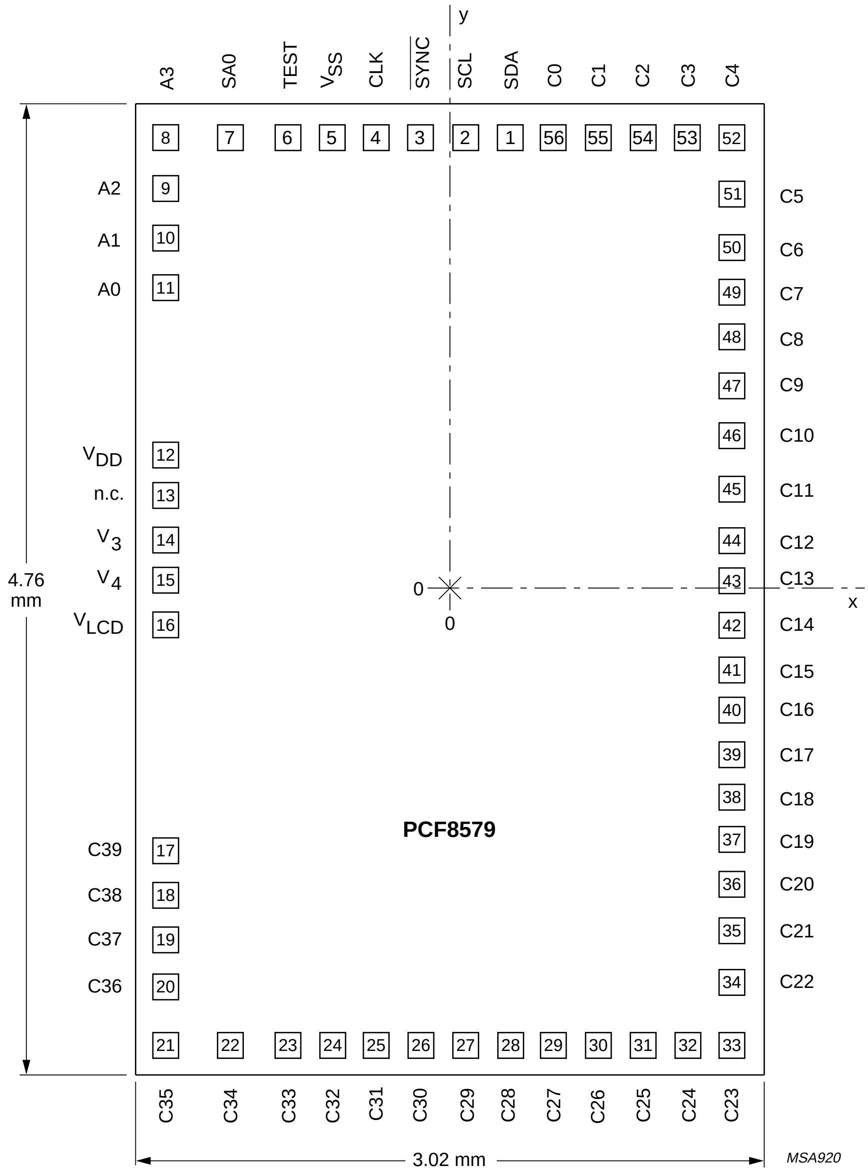


Fig.23 Example of single plane wiring, single screen with 1 : 32 multiplex rate (PCF8578 in row driver mode).

15 CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 14.37 mm^2.
Bonding pad dimensions: 120 µm × 120 µm.
Gold bump dimensions (if ordered): 94 × 94 × 25 µm.
The numbers given in the square boxes refer to the pad number.

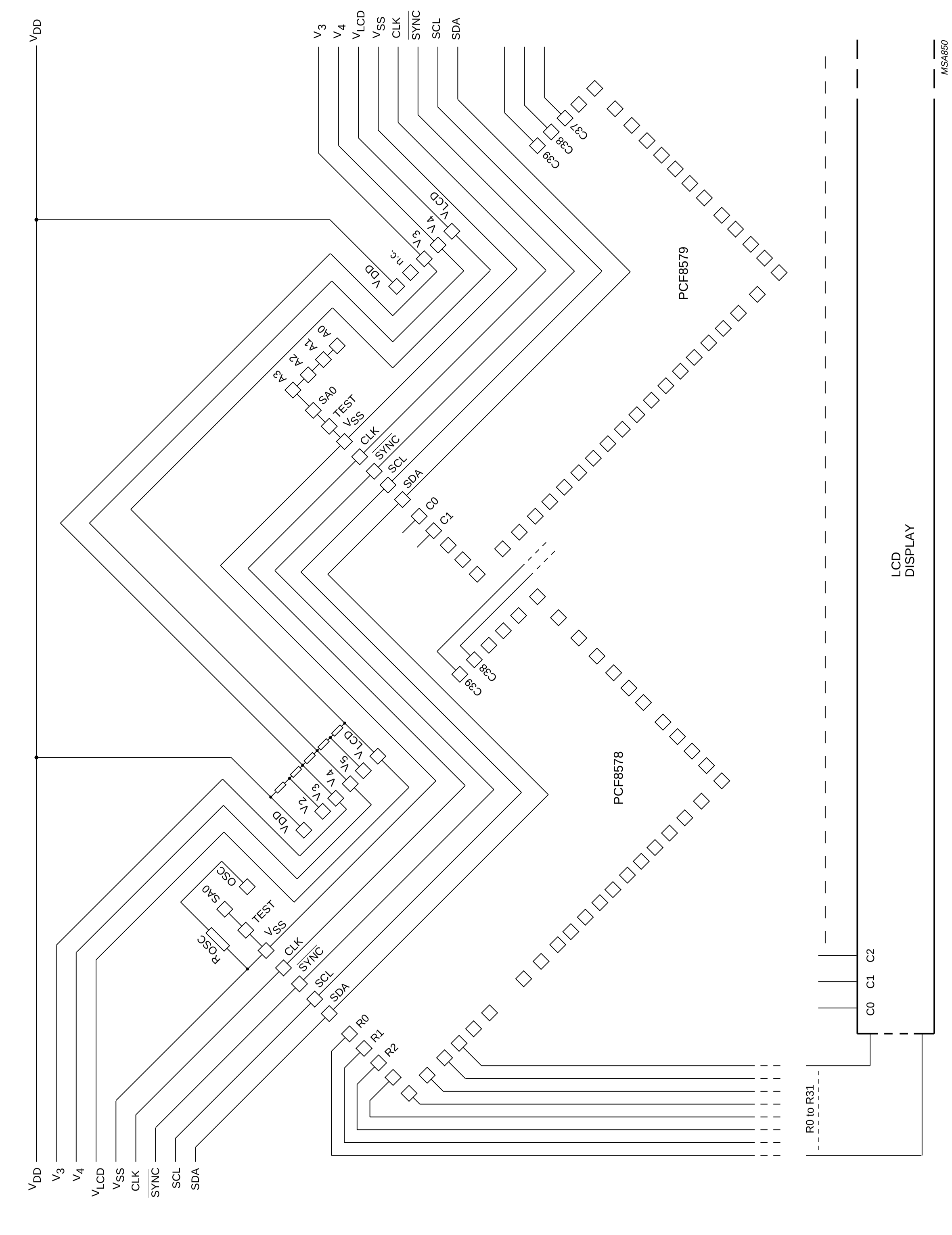
Fig.24 Bonding pad locations.

Table 12 Bonding pad locations (dimensions in μm); all x/y coordinates are referenced to centre of chip, see Fig.24.

PAD NUMBER	SYMBOL	x	y	PINS	
				VSO56	LQFP64
1	SDA	252	2142	1	7
2	SCL	48	2142	2	8
3	$\overline{SYNC}$	–156	2142	3	9
4	CLK	–360	2142	4	10
5	V_{SS}	–564	2142	5	11
6	TEST	–786	2142	6	12
7	SA0	–1032	2142	7	13
8	A3	–1314	2142	8	14
9	A2	–1314	1920	9	16
10	A1	–1314	1716	10	17
11	A0	–1314	1512	11	18
12	V_{DD}	–1314	708	12	20
13	n.c.	–1314	504	13	21
14	V_3	–1314	300	14	22
15	V_4	–1314	96	15	23
16	V_{LCD}	–1314	–108	16	24
17	C39	–1314	–1308	17	30
18	C38	–1314	–1512	18	31
19	C37	–1314	–1716	19	32
20	C36	–1314	–1920	20	33
21	C35	–1314	–2142	21	35
22	C34	–1032	–2142	22	36
23	C33	–786	–2142	23	37
24	C32	–564	–2142	24	38
25	C31	–360	–2142	25	39
26	C30	–156	–2142	26	40
27	C29	48	–2142	27	41
28	C28	252	–2142	28	42
29	C27	498	–2142	29	43
30	C26	702	–2142	30	44
31	C25	906	–2142	31	45
32	C24	1110	–2142	32	46
33	C23	1314	–2142	33	47
34	C22	1314	–1830	34	48
35	C21	1314	–1570	35	49
36	C20	1314	–1326	36	50
37	C19	1314	–1122	37	51
38	C18	1314	–918	38	52

PAD NUMBER	SYMBOL	x	y	PINS	
				VSO56	LQFP64
39	C17	1314	–714	39	53
40	C16	1314	–510	40	54
41	C15	1314	–306	41	55
42	C14	1314	–102	42	56
43	C13	1314	102	43	57
44	C12	1314	306	44	58
45	C11	1314	510	45	59
46	C10	1314	714	46	60
47	C9	1314	918	47	61
48	C8	1314	1122	48	62
49	C7	1314	1326	49	63
50	C6	1314	1566	50	64
51	C5	1314	1830	51	1
52	C4	1314	2142	52	2
53	C3	1110	2142	53	3
54	C2	906	2142	54	4
55	C1	702	2142	55	5
56	C0	498	2142	56	6
–	n.c.	–	–	–	15, 19, 21, 25 to 29, 34

16 CHIP-ON GLASS INFORMATION

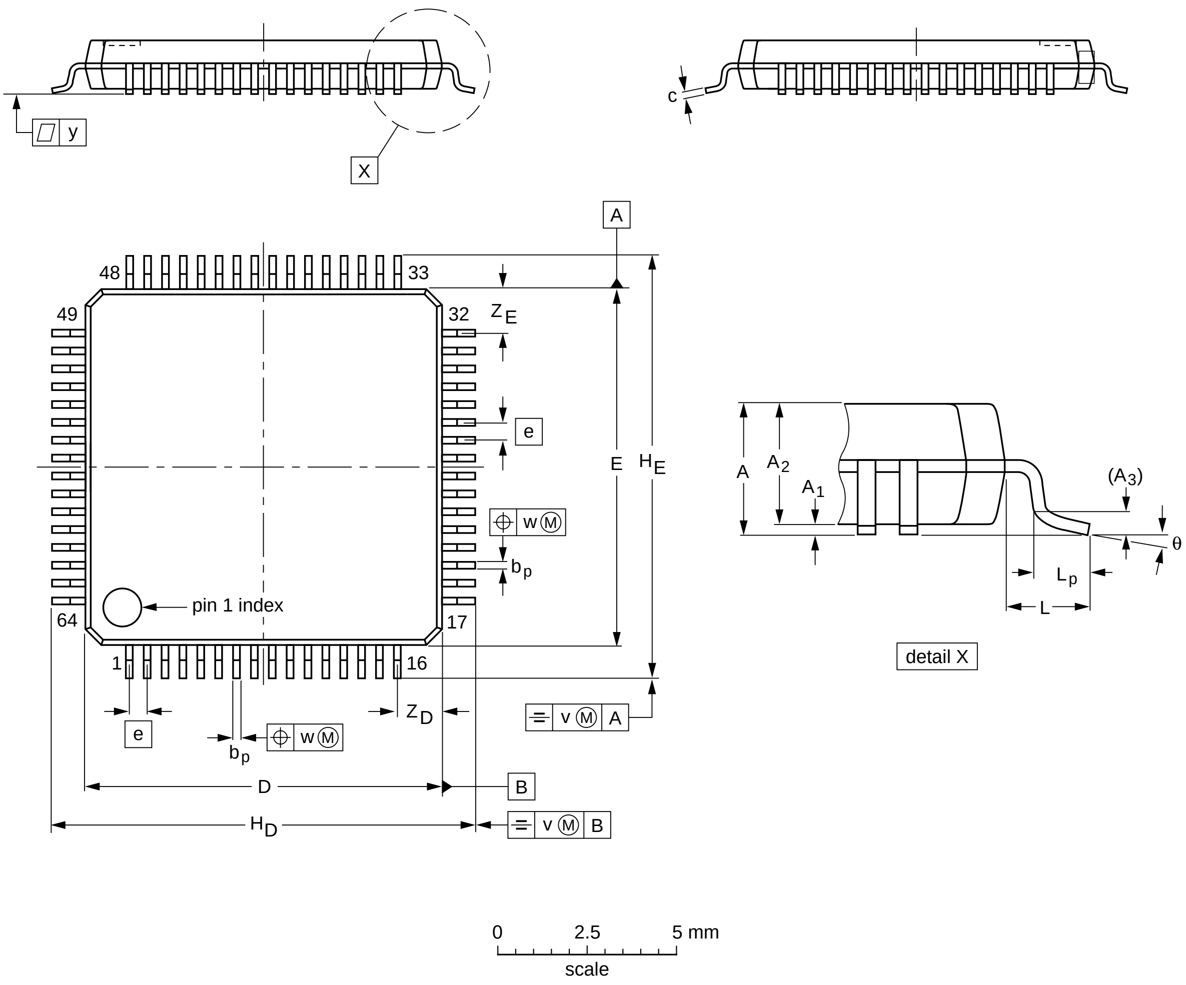


If inputs SA0 and A0 to A3 are left unconnected they are internally pulled-up to V_{DD}.

Fig.25 Typical chip-on glass application (viewed from underside of chip).

17 PACKAGE OUTLINES

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm SOT314-2



DIMENSIONS (mm are the original dimensions)

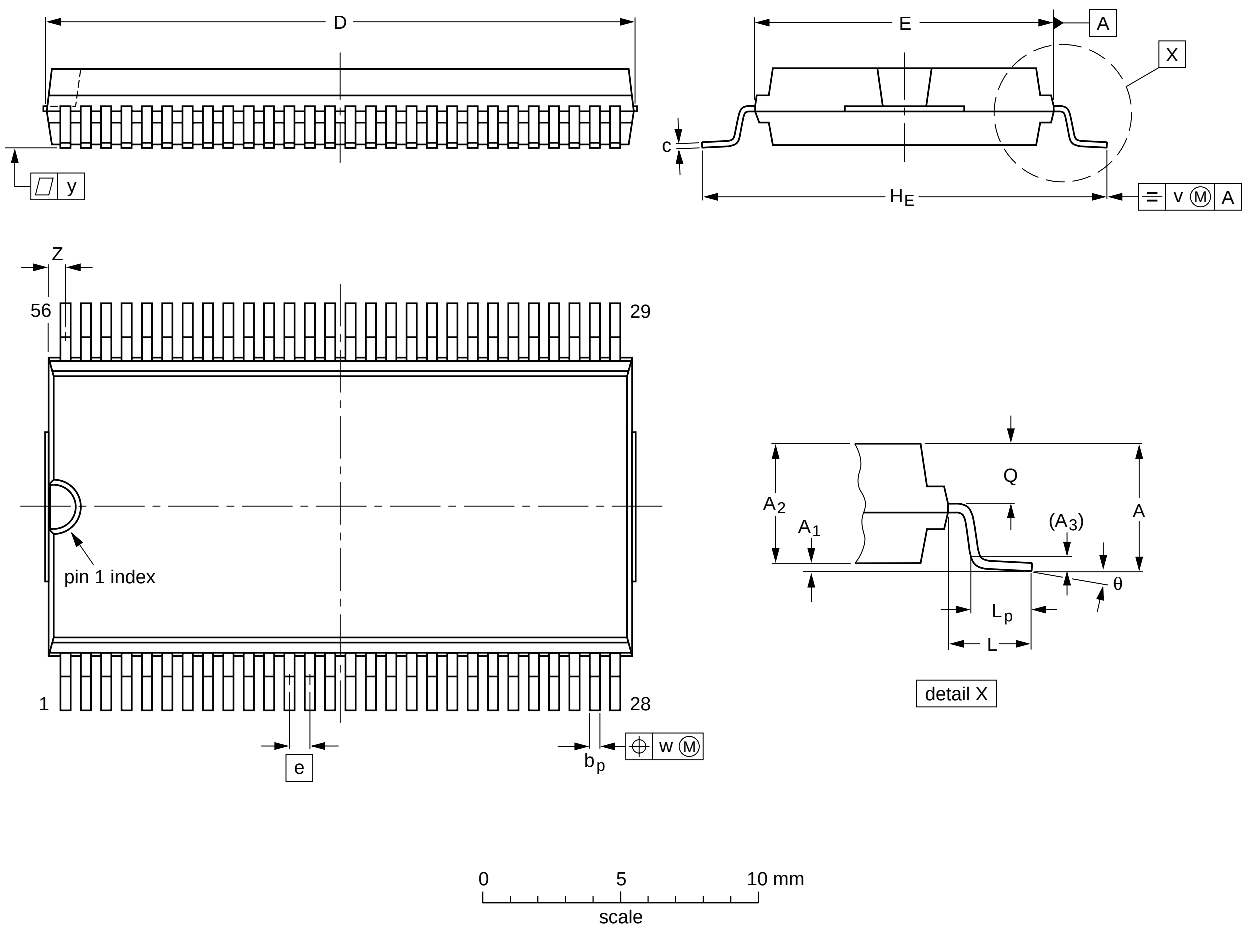
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

VSO56: plastic very small outline package; 56 leads | **SOT190-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.65 21.35	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7° 0°
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0055	0.85 0.84	0.44 0.43	0.0295	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

Notes

1. Plastic or metal protrusions of 0.3 mm (0.012 inch) maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT190-1						~~97-08-11~~ 03-02-19

18 SOLDERING

18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

18.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, SSOP-T[3], TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

19 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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